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10/587,596	04/24/2007	Wolfgang Schnitt	DE04 0034 US1	2386

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EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
12/10/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/587,596	SCHNITT ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2, 3, and 6 – 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Woo et al. (US 5,408,130).

a. Regarding claim 8, **Woo discloses an integrated circuit chip** (e.g. figures 3 and 5) **comprising:**

at least one integrated circuit (e.g. within layer 12, as disclosed in col. 3, lines 41 - 46); **and**

an integrated electrostatic discharge protection device, the electrostatic discharge protection device comprising:

an insulating layer (layer 12) **disposed on a substrate layer** (substrate 10), **the insulating layer of an electrically insulating material to form a base layer of a toroidal spark gap cavity** (layer 12 disclosed to be a dielectric layer in col. 3, lines 40 and 42. Toroidal spark gap cavity formed by opening 19 and surrounding layers, as seen in figures 3 - 5, and further disclosed in col. 9, lines 16 - 25);

a first electrically conductive layer disposed on the insulating layer (e.g. conductive layer 18, disclosed in col. 4, line 7), **the first electrically**

conductive layer of a first electrically conductive material (e.g. as disclosed in col. 4, lines 7 - 9, with reference to col. 3, lines 52 - 58) **to form a circumferential electrode with an outer side wall to define a window** (window 19) for the toroidal spark gap cavity (e.g. circumference of toroid shown with respect to figure 5);

a dielectric layer disposed on the first electrically conductive layer, the dielectric layer of a dielectric material to form a cover layer of the toroidal spark gap cavity (dielectric layer 20, disclosed in col. 4, line 14); **and**

a second electrically conductive layer partially disposed directly on the dielectric layer and extending into the window for the toroidal spark gap cavity to be partially disposed directly on the insulating layer (second electrically conductive layer 24, disclosed in col. 5, line 23), **the second electrically conductive layer of a second electrically conductive material to form a center electrode with an inner side wall that is laterally separated from the outer side wall of the first conductive layer by the toroidal spark gap cavity** (e.g. as seen in figures 3 and 5).

b. Regarding claim 2, **Woo discloses the integrated circuit chip of claim 8, further comprising a passive component selected from the group comprising resistors, capacitors, and inductors** (disclosed in col. 3, line 45).

c. Regarding claim 3, **Woo discloses the integrated circuit chip of claim 8, wherein the first electrically conductive material is polysilicon** (col. 3, line 55).

d. Regarding claim 6, **Woo discloses the integrated circuit chip of claim 8, wherein the substrate material is selected from the group comprising silicon, glass and a ceramic material** (col. 3, lines 31 - 35).

e. Regarding claim 7, **Woo discloses a method of fabricating an integrated circuit chip comprising an integrated circuit and an electrostatic discharge protection device** (e.g. figures 1 - 5), **the method comprising:**

providing a semiconductor substrate (substrate 10),

depositing an insulating layer on the semiconductor substrate (dielectric layer 12),

depositing a first electrically conductive layer of a first electrically conductive material on said insulating layer (e.g. conductive layer 18, disclosed in col. 4, line 7),

depositing a dielectric layer of a dielectric material directly on said first electrically conductive layer (dielectric layer 20, disclosed in col. 4, line 14),

etching the dielectric layer to form a window for a center electrode (as disclosed in col. 4, lines 36 – 37),

etching the first electrically conductive layer under the dielectric layer to form a toroidal spark gap cavity with a vertical gap between the insulating layer and the dielectric layer, wherein an exposed surface of the first electrically conductive layer forms a circumferential electrode (e.g. as seen in figures 2 and 5, and disclosed in col. 4, lines 37 – 41),

depositing a layer of a second electrically conductive layer (second electrically conductive layer 24, disclosed in col. 5, line 23) **through the window to form the center electrode mechanical contact with the insulating layer** (e.g. as seen in figure 4, the second electrically conductive layer 24 is deposited through the window 19, and in mechanical contact with the insulating layer 12) **and to seal the toroidal spark gap cavity with a lateral gap between the first and second electrically conductive layers** (e.g. as seen in figure 3, the second electrically conductive layer 24 seals the gap 19 by being in contact with layer 20),

connecting the center electrode to input circuit paths to be protected from electrostatic discharge (e.g. as seen in figures 4 and 5, the center electrode 24 extends along the device direction, and is also disclosed to be in contact with an electrode of a transistor, as disclosed in col. 7, lines 1 – 2), and

connecting the circumferential electrode to an electrostatic discharge path comprising either a connection to a circuit ground or a circuit supply voltage (col. 6, lines 26 – 31 disclose connecting the first

electrically conductive layer 18 comprising the circumferential electrode to a circuit ground).

f. Regarding claim 9, **Woo discloses the integrated circuit chip of claim 8, wherein the dielectric layer extends at least partially over the window of the toroidal spark gap cavity formed by the first electrically conductive layer** (e.g. as seen in figure 3, the dielectric layer 20 extends over the window area of the toroidal spark gap cavity 19 in the region of 19a).

g. Regarding claim 10, **Woo discloses the integrated circuit chip of claim 9, wherein the dielectric layer is vertically separated from the insulating layer by the toroidal spark gap cavity** (e.g. as seen in figure 3, the dielectric layer 20 is separated from the insulating layer 12 by the gap cavity 19).

h. Regarding claim 11, **Woo discloses the integrated circuit chip of claim 8, further comprising means for electrically connecting the center electrode to input circuit paths to be protected from electrostatic discharge** (e.g. as seen in figure 5, the center electrode 24 extends in a direction parallel to layer 18, and therefore this extension of the conductive layer 24 may be considered the "*means for electrically connecting the center electrode to input circuit paths to be protected for electrostatic discharge*". Furthermore, it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus

is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114).

i. Regarding claim 12, **Woo discloses the integrated circuit chip of claim 8, further comprising means for electrically connecting the circumferential electrode to an electrostatic discharge path comprising a connection to a circuit ground or a circuit supply voltage** (e.g. as seen in figure 5, the center electrode 24 extends in a direction parallel to layer 18, and therefore this extension of the conductive layer 24 may be considered the *"means for electrically connecting the circumferential electrode to an electrostatic discharge path comprising a connection to a circuit ground or a circuit supply voltage*". Furthermore, it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114).

j. Regarding claim 13, **Woo discloses the integrated circuit chip of claim 8, wherein the toroidal spark gap cavity is an annular cavity defined by the inner side wall of the second electrically conductive layer, the outer side wall of the first electrically conductive layer, the base layer of the insulating**

layer, and the cover layer of the dielectric layer (e.g. as seen in figures 3 and 5).

k. Regarding claim 14, **Woo discloses the method of claim 7, wherein depositing the second electrically conductive layer further comprises at least partially depositing the second electrically conductive layer on and in direct contact with the dielectric layer** (as seen in figures 3 and 4, the second electrically conductive layer 24 is on and in direct contact with the dielectric layer 20).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al. in view of Momodomi (US 4,881,113, prior art of record). **Woo discloses the integrated circuit chip of claim 8, but is silent with respect to disclosing that the second electrically conductive material is aluminum. However, Woo discloses that the second conductive layers may comprise metal** (col. 5, lines 30 - 35).

Momodomi discloses an integrated circuit chip may comprise electrically conducive layers, wherein electrically conductive material is aluminum (col. 3, lines 1 – 2 disclose the second electrode 18 to be aluminum Al. Col. 6, lines 30 – 32 also disclose that it may be made from Mo and W instead of Al).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Woo such that the second conductive layer was formed of aluminum since Woo discloses the layer to be a metal, but is simply silent with respect to the material, and Momodomi discloses that aluminum may be used as conductive layers in integrated circuit devices. Furthermore, it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use aluminum as the second conductive layer material since it is very conductive, inexpensive, and may be formed using predictable, known methods such as evaporation.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Woo et al. in view of Igel et al. (US 6,204,549 B1, prior art of record). **Woo discloses the integrated circuit chip of claim 8, as cited above, but is silent with respect to disclosing the spark gap cavity contains a noble gas for reducing the breakdown voltage of the electrostatic discharge protection device. Woo does discloses that the spark gap cavity may exist without a spacer layer** (col. 9, lines 16 – 25)

Igel teaches that a cavity filled with a noble gas may be used in voltage protection devices (col. 2, lines 38 – 40).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the spark gap cavity of Woo such that it is filled with a noble gas, since Woo teaches the cavity may be empty (i.e. not filled with a spacer) when the dimensions become small (col. 9, lines 16 - 25), and Igel teaches that noble gas can be used to fill cavities between electrodes. One would be motivated to make such a modification since a noble gas filled cavity allows one to control the breakdown voltage between the electrodes, as discussed by Igel (col. 2, lines 44 – 47), as well as not being reactive with the electrodes so that there is no corrosive effects.

Response to Arguments

7. Applicant's arguments with respect to claims 7 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
December 5, 2009